FLASH MEMORY CELL AND METHODS FOR FABRICATING SAME

FIELD OF INVENTION

[0001] The present invention relates to semiconductors. More specifically, the present invention relates to a split gate flash memory cell for split gate flash memories and embedded split gate flash memories, and methods for fabricating such a memory cell.

BACKGROUND OF THE INVENTION

[0002] Split gate flash memory cells for split gate flash memories and embedded split gate flash memories are typically fabricated using numerous etching processes. A substantial number of these etching processes are critical for fabricating the structures of the memory cells. The numerous etching processes create serious oxide loss in the shallow trench isolation (STI) regions. To avoid serious oxide loss, the floating gate etching window must be very narrow and is therefore, not suitable for mass production.

[0003] In addition, a number of these etching processes are used for forming the floating gates of the cells. Due to all of these etching processes, an oxide micro-mask may be formed in the floating gate poly etching process, which presents a serious bridging issue.

SUMMARY OF INVENTION

[0004] A flash memory cell is disclosed herein where the cell comprises a floating gate having sharp, upwardly flared corners.

[0005] The flash memory cell may also comprise a cap of dielectric material covering the floating gate, wherein the cap has a substantially square or substantially rectangular cross sectional shape.

[0006] The flash memory cell may further comprise a dielectric Vss spacer covering a generally planar side wall defined by the floating gate and the cap.

[0007] A method of making the flash memory cell is also disclosed herein. The method comprises providing a substrate of semiconductor material; forming a mask film over the substrate; defining a trench in the mask film; at least partially filling the trench with a first film of electroconductive material; and etching back a portion of the first film of electroconductive material to partially form the floating gate with the sharp, upwardly flared corners.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] FIGS. 1A-1D, 2A-2H, 3A-3E, 4A-4G, 5A-5C, 6A-6C, and 7A-7C are plan and cross-sectional views illustrating the method of the present invention, wherein the cross-sectional views of FIGS. 1A-1D and 2A depict a first vertical plane through a substrate on which the memory cell of the invention is fabricated and the cross-sectional views of FIGS. 2B-2H, 3A, 3B, 3D, 3E, 4A-4D, 4F, 5A-5C, 6A-6C, and 7A-7C depict a second vertical plane through the substrate that is perpendicular to the first vertical plane.

DETAILED DESCRIPTION OF THE INVENTION

[0009] The present invention is an improved split gate flash memory cell for split gate flash memories and embedded split gate flash memories, which is fabricated in method that utilizes a significantly reduced number of etching processes, and includes only a single critical etching process. As will become apparent further on, the method of the invention does not consume shallow trench isolation (STI) oxide and bridging issues are eliminated, as no floating gate etching process is utilized.

[0010] The method of the invention commences with STI processing of semiconductor substrate 10, as shown in FIGS. 1A-1D. The semiconductor substrate 10 is not limited to a particular type and may be those generally used in a semiconductor memory device, examples thereof including an element semiconductor, such as Si and Ge, and a compound semiconductor, such as GaAs, InGaAs and ZnSe.

[0011] As shown in FIG. 1A, film 12 of dielectric material is formed over an active region of substrate 10. Film 12 may comprise, without limitation, a nitride such as SiN, deposited by low pressure chemical vapor deposition (LPCVD). Film 12 may be formed to a thickness which ranges between about 1200 Angstroms (A) and about 1800A. In one illustrative embodiment, film 12 may be formed to a thickness of about 1620A. A thermal oxide film (not shown) may be disposed between substrate 10 and film 12. The thermal oxide film may have a thickness of about 120 A to about 170 A.

[0012] Substrate 10 is then STI masked and unmasked portions of film 12 and the underlying areas of substrate 10 are etched to form shallow trenches 13 (only one is shown for purposes of clarity), as shown in FIG. 1B. Etching may be accomplished using, for example, reactive ion etching (RIE). Shallow trenches 13 may have a depth between about 2000A and about 6000A.

[0013] Shallow trenches 13 are then filled with a suitable dielectric isolation material, such as silicon oxide by forming film 14 of the dielectric material conformally over substrate 10, as shown in FIG. 1C. Film 14 may be formed using, for example, high density plasma chemical vapor deposition (HDP CVD) or low pressure chemical vapor deposition (LPCVD).

[0014] Substrate 10 is subsequently planarized using film 12 as a stop layer. Planarizing may be accomplished with a chemical mechanical polishing (CMP) process. After planarizing, film 12 is removed (a nitride strip may be used, for example, when film 12 is made of SiN) to form STI regions 15 which extend partially above the surface of substrate 10, as shown in FIG. 1D.

[0015] Once STI processing has been completed, a pad oxide on which the split floating gate structure of the memory cell will reside, is formed over an active region of substrate 10. More specifically, in FIG. 2A which is a cross-sectional view through STI region 15 and FIG. 2B which is a sectional view through line 2B-2B of FIG. 2A, film 16 of dielectric material (the pad oxide) is formed over an active region of substrate 10. In embodiments where substrate 10 is composed of Si, dielectric film 16 may comprise a thermally grown oxide such as silicon dioxide. Dielectric film 16 is typically formed to a thickness which ranges

between about 80A and about 180A. In one illustrative embodiment, dielectric film16 may be formed to a thickness of about 120A.

[0016] FIG. 2C illustrates substrate 10, as shown in FIG. 2B, after floating gate mask film 17 (FLG mask 17) has been formed thereover. In one embodiment, FLG mask 17 may be composed of SiN. Such a FG mask 17 may be formed using CVD, for example. FLG mask 17 is typically formed to a thickness which ranges between about 3500A and about 4500A . In one illustrative embodiment, FLG mask 17 may be formed to a thickness of about 4000A.

[0017] In FIG. 2D, photoresist mask 18 is formed over substrate 10 and in FIG. 2E, unmasked portions of FLG mask 17 are removed thereby forming a pair of spaced apart trenches 19. The unmasked portions of the FLG mask 17 may be removed using an etch process, such as RIE.

[0018] As shown in FIG. 2F, exposed portions of the dielectric film 16 at the bottom of trenches 19 are removed using, for example, a wet etch process that utilizes dilute HF acid. The dielectric film removal process exposes the underlying portions of substrate 10 at the bottom of trenches 19.

[0019] In FIG. 2G, coupling films 20a and 20b composed of a dielectric material are formed over the exposed portions of the substrate 10 at the bottom of the trenches 19. In embodiments where the substrate 10 is composed of Si, the coupling films 20a and 20b may comprise silicon dioxide, which may be thermally grown on the substrate 10. The coupling films 20a and 20b are typically formed to a thickness which ranges between about 60A and about 100A. In one

illustrative embodiment, the coupling films 20a and 20b may each be formed to a thickness of about 80A.

[0020] In FIG. 2H, the trenches 19 are filled with conformal film 21 of electroconductive material, such as doped polysilicon. Electroconductive film 21 may be formed using conventional methods including, without limitation, CVD and physical vapor deposition (PVD) utilizing sputtering methods employing suitable source materials. In one embodiment, electroconductive film 21 may have a thickness of about 2200A.

[0021] FIGS. 3A-3E illustrate a first method for forming the split floating gate structure starting with substrate 10 shown in FIG. 2H. In FIG. 3A, electroconductive film 21 is partially removed using a conventional etch-back process to form floating gates 22a and 22b with sharp, upwardly flared corners 23a and 23b respectively. In one exemplary embodiment, the floating gates 22a and 22b may have a thickness T_1 of about 600A. Next, patterned mask film 18 is formed over substrate 10 as collectively shown in FIGS. 3B and 3C. Patterned mask film 18 may be a layer of photoresist. In FIGS. 3D and 3E, the unmasked areas of floating gates 22a and 22b are removed down to STI regions 15 to electrically isolate each unit cell. This may be accomplished using a plasma etching process. Patterned mask film 18 is then striped from substrate 10.

[0022] FIGS. 4A-4G illustrate a second method for forming the split floating gate structure starting with substrate 10 shown in FIG. 2H. In FIG. 4A, electroconductive film 21 is partially removed using a conventional etch-back process to recess the electroconductive film 21 below the surface of FLG mask

film 17. In one exemplary embodiment, each recess R may be about 800A. After etch-back, electroconductive film 25 is conformally formed over substrate 10, shown in FIG. 4B. In FIG. 4C, electroconductive films 21 and 25 are partially removed using a conventional etch-back process to form floating gates 22a and 22b with sharp, upwardly flared corners 23a and 23b provided by electroconductive film spacers 25a and 25b formed from the partially removed electroconductive film 25. In one exemplary embodiment, floating gates 22a and 22b made according to the second method may have a thickness T_2 of about 600A. Next, patterned mask film 24 is formed over substrate 10 as collectively shown in FIGS. 4D and 4E. As in the first method, mask film 24 may be a layer of photoresist. As collectively shown in FIGS. 4F and 4G, the unmasked areas of floating gates 22a and 22b are subsequently removed down to STI regions 15 to electrically isolate each unit cell using a plasma etching process and patterned mask film 24 is then striped from substrate 10.

[0023] Once floating gates 22a and 22b have been formed (using either one of the two methods described above), a protective cap 26 of dielectric material is formed on each floating gate 22a and 22b using the exemplary method shown in FIGS. 5A-5C. Specifically, in FIG. 5A, a conformal film of dielectric material, such as silicon oxide, is formed over substrate 10 using, for example, HDP CVD, such that it fills the spaces above floating gates 22a and 22b. The film is then planarized such that the only remaining portions of the film are the caps 26 (filling trenches 19). As can be seen in the cross-sectional view of FIG. 5A, the caps 26 each have a substantially rectangular or square shape. The conformal

film of dielectric material may be formed using HDP CVD. The conformal film of dielectric material may be planarized using a CMP process that utilizes FLG mask 17 as a stop layer.

[0024] The FLG mask 17 and dielectric film 16 are then removed from substrate 10, as shown in FIG. 5B. Removal of these films may be accomplished using a wet chemical etch process that employs hot H_3PO_4 acid and dilute HF acid, respectively.

[0025] Finally, as shown in FIG. 5C, conformal film 27 of dielectric material is formed over substrate 10 and areas thereof are masked with mask layer 28. In one embodiment, conformal film 27 may be silicon oxide formed to a thickness of about 800A using a thermal growing process. Mask layer 28 may be a patterned layer of photoresist.

[0026] FIGS. 6A-6C illustrate an exemplary method for forming Vss spacers. In FIG. 6A, the unmasked areas of film 27 have been removed (followed by the removal of the mask layer 28) and a conformal tunneling film 29 has been subsequently formed over substrate 10. The unmasked areas of film 27 may be removed using an etching process, such as a wet chemical etch process employing dilute HF acid. In one embodiment, tunneling film 29 may be silicon oxide formed to a thickness of about 155A using, for example, a high temperature oxide process.

[0027] In FIG. 6B, mask layer 30 is formed over substrate 10. Mask layer 30 may be a patterned layer of photoresist.

[0028] In FIG. 6C, Vss spacers 32a and 32b have been formed along opposing side walls of floating gates 22a and 22b and corresponding caps 26 by removing the unmasked portions of tunneling film 29 and corresponding portions of film 27 from Vss area 31 and caps 26. The mask layer 30 has also been removed. The removal of these unmasked portions of tunneling film 29 and film 27 may be accomplished using a plasma etching process. As can be seen, Vss spacers 32a and 32b are formed by remaining unmasked portions of the tunneling film 29 and the film 27.

[0029] FIGS. 7A-7C illustrate an exemplary method for forming electroductive Vss plug and electroductive wordline spacers. In FIG. 7A, a conformal, electroconductive film 33 has been formed over substrate 10. In one embodiment, the electroconductive film 33 may be a film of doped polysilicon having a thickness of about 1800A.

[0030] In FIG. 7B, the electroconductive film 33 has been partially removed to form electroconductive Vss plug 34 between Vss spacers 32a and 32b, and electroconductive wordline spacers 35 along the dielectrically coated outer side walls of floating gates 22a and 22b and caps 26. The partial removal of electroconductive film 33 can be accomplished using an etch-back process such as plasma etching.

[0031] In FIG. 7C silicide films 36 have been formed over Vss plug 34 and wordline spacers 35a and 35b and composite spacers 37a and 37b have been formed on the outer side walls of the wordline spacers 35a and 35b, to complete

the memory cell. The silicide films 36 may be formed using a salicide process. In one embodiment, the silicide films 36 may comprise cobalt silicide films.

[0032] The composite spacers 37a and 37b may be formed by depositing a conformal SiN film over substrate 10. The SiN film may have a thickness of about 300 A and be formed using LPCVD. Next, a tetraethyl orthosilicate (TEOS) film is formed over the SiN film. The TEOS film may have a thickness of about 1000A and be formed using LPCVD. The TEOS and SiN films are separately etched to form spacers 37a and 37b. Each etching process may be accomplished using a dry plasma etch process.

[0033] As can be seen in FIG. 7C, floating gates 22a and 22b are electrically associated with a common source region 38 formed in substrate 10 and wordline spacers 35a and 35b are electrically associated with respective drain regions 40a and 40b formed in the substrate 10. Channel regions 42a and 42b are created in substrate 10 between common source region 38 and respective drain regions 40a and 40b when appropriate electrical biases are applied thereto during cell programming. The sharp upwardly flared corner tip adjacent the Vss plug 34 of each floating gate 22a and 22b, increases the coupling area, which increases the capacitance between the floating gates 22a and 22b and common source region 38. The increased capacitance increases the programming speed of the memory cell, i.e., the writing and erasing speeds of the cell. The square or rectangular shape caps 26 provide for the square wordline spacers 35a and 35b. The square wordline spacers 35a and 35b, in turn, increase the processing window for the L shaped spacers 37a and 37b and the salicide process. The elongated Vss spacers

32a and 32b are thinner than conventional Vss spacers, thereby increasing coupling efficiency.

[0034] While the foregoing invention has been described with reference to the above, various modifications and changes can be made without departing from the spirit of the invention. Accordingly, all such modifications and changes are considered to be within the scope of the appended claims.